Gold Contacts to Semiconductor Devices

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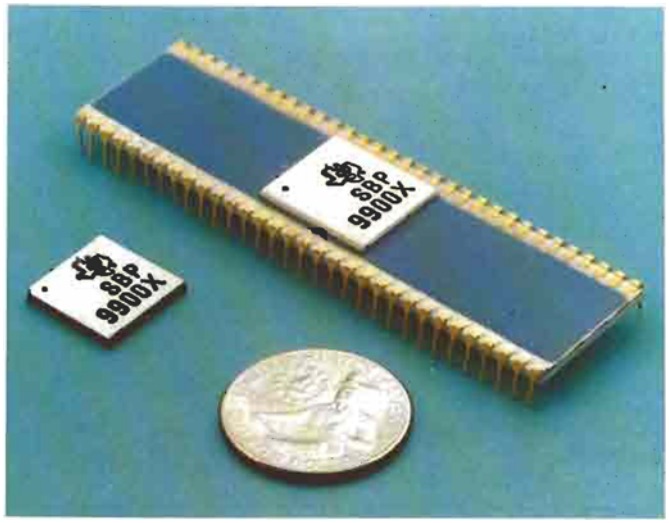
The electronics revolution led by computers and microprocessors is based on the silicon integrated circuit. Gold contacts play a key role in the fabrication of integrated circuits. For microwave devices and integrated circuits made from compound semiconductors such as gallium arsenide, gold metallization is used for both ohmic and rectifying contacts.

The world-wide explosion in information-processing and in automation for industry is a direct result of the widespread availability of the integrated circuits contained on small 'chips' of silicon and other semiconductors. In this highly competitive arena, gold plays a key role. Gold as a material for making contacts to semiconductors has made a greater contribution than any other metal to advances in integrated circuit development. The present computer and micro-processor based technology that rests on the availability of low-cost and reliable electronic components can trace its present high-performance capabilities to the utilization of gold contacts.

Other articles in *Gold Bulletin* have been concerned with the application of gold in solar cells (1) and in thyristors (2). In this review, we consider gold as the contact, the medium through which electrical signals generated within semiconductor devices are transmitted to the outside world. As we will see, gold serves in many capacities from that of a 'weld' material formed in low temperature processing to that of the rectifying contact in the most-advanced, high-speed devices used in microwave and high-frequency devices. In the field of physics research, the application of gold in semiconductor devices has been the key element in detectors of nuclear radiation which have dominated low-energy nuclear physics for nearly two decades.

In electronic systems the prime objective is to minimize voltage losses in the current carrying connections. It is also imperative that the electrical properties of the connectors do not change when exposed to air. In these respects, gold is by far the outstanding candidate and is the immediate choice in metallization schemes. Even a cursory examination of a commercial microprocessor will reveal that the external contacts on the package are gold-plated to ensure against degradation in the operating environment (Figure 1).

Fig. 1 **Integrated circuits that have been covered and packaged. The exterior contact leads have been gold plated for reliability in electrical connection to the microcomputer module. (Photo courtesy of Texas Instruments, Dallas, Texas)**



Ohmic Contacts to Silicon Chips

In device fabrication silicon chips must be provided with ohmic contacts not only to the package leads, but also to the pads on which they are mounted. Gold is involved in both these operations so that the processes which occur in bonding between gold and silicon are of considerable importance.

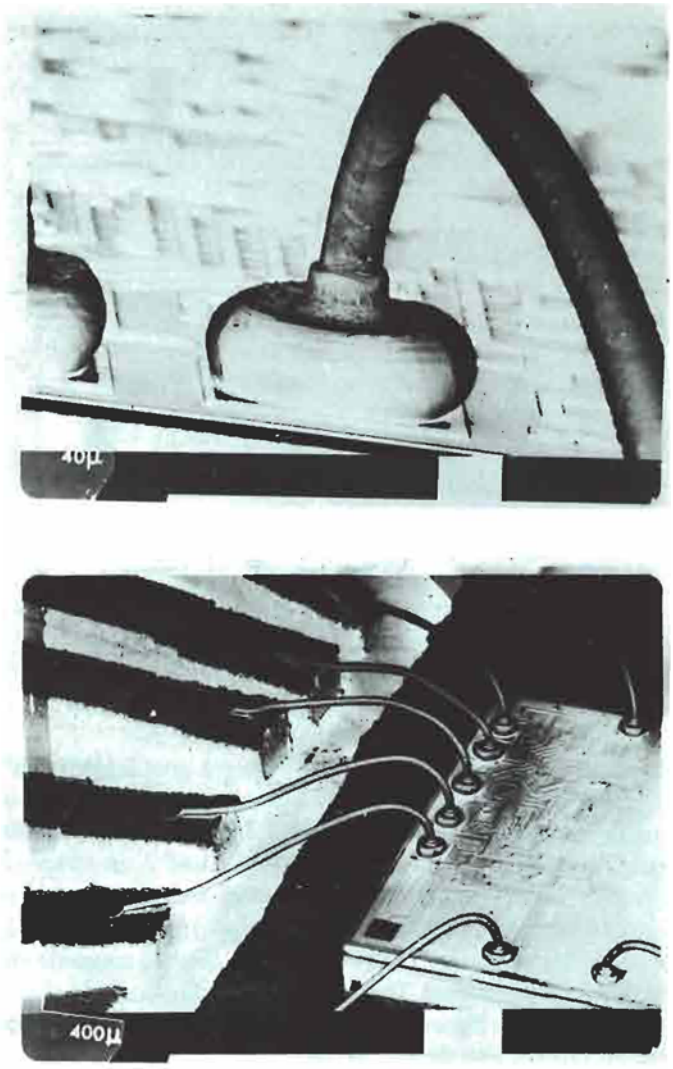
Wire Bonding

Although not immediately obvious, the ductility of gold ensures its use in the wire bonds within the package that make the connection between the silicon chip and the outer contacts. Figure 2 shows in the upper portion an expanded view of the gold wire that has been bonded to the metallized pads on the silicon chip. In production, the gold wire is passed through a capillary and a ball is formed at the end. The silicon chip is heated to around 250°C (less than the melting point of the Au-Si eutectic) and when the ball is placed in contact with the bonding pad on the chip, pressure from the capillary deforms the ball into the shape of a nail head which bonds with the pad and establishes an ohmic contact with the silicon. After this thermo-compression bonding step, the capillary head is raised and repositioned so that it can be bonded to the package lead. The gold wire thus makes an electrical connection between the silicon bonding pad and the assembly package leads (Figure 2, lower portion). The ductility of the gold wire is of critical importance, not only in production operation but also in the subsequent quality assurance vibration and adherence tests.

Base Contacts to Silicon Chips

In the production of a silicon integrated circuit chip — typically a 5 × 5 mm by 250 μm thick section — the majority of the processing viz. all the oxidation, photolithography, ion implantation, diffusion and other steps, is carried out on a 7.5 to 10 cm diameter slice or wafer of silicon. This is then cut into the 5 × 5 mm chips and

Fig. 2 A view of the gold wires bonded to a silicon integrated circuit chip (upper portion) and the connections (lower portion) to the contact leads of the package. (Photo courtesy of SGS-ATES Electronic Components, Milan, Italy)



placed on the gold-plated mounting pad in the package such as shown in Figure 3. It is of utmost importance that the simple step of attaching the silicon chip to the bottom mounting plate be carried out without disturbing any of the previous processing procedures. In the early 1950's when germanium diodes were assembled in glass packages with spring wire top contacts, the bottom attachment was made with a gold paste epoxy. This thermosetting resin attachment process was used for nearly a decade while prices of the germanium diode dropped a thousand-fold from about US $50 per diode to US $0.07 per diode. These epoxy resins are not suitable in present integrated circuit applications because the contact resistance is high and the epoxy degrades under the heat treatment required for sealing the final package. In order to find a replacement it was necessary to find a large area attachment procedure that gave reliable, stable and low resistance contact to metal. It is common practice in the last stages of processing the wafer — when the metal contacts and interconnects have been deposited — to use a final process temperature of no more than 450 to 500°C to form the metallization contacts. Therefore the attachment of the silicon chip to the mounting plate must be carried out at substantially reduced temperatures.

It is at this point that one takes advantage of the remarkably low gold-silicon eutectic temperature. The reduction in the melting point of an alloy of gold as compared to those of the constituent elements has been known since 1763 (3). However the combination of gold with a melting temperature of 1 063°C and silicon which melts at 1 412°C leads to a eutectic melting point of 363°C (4, 5). This represents one of the most dramatic reductions in the melting point of any combination of the common elements. The equilibrium phase diagram shown in Figure 4 illustrates the precipitous drop in the melting point as the gold-silicon alloy composition nears that of 19 atomic per cent of silicon in gold (the eutectic composition). The low eutectic temperature is the key feature in the choice of gold-plated metal pads for the bottom silicon attachment. The gold-silicon eutectic temperature is about 100°C below the final temperatures used in processing the wafer and hence the attachment step does not perturb the device configuration.

Mechanism of Gold-Silicon Eutectic Bonding

One would not expect that placement of the silicon chip on a gold film would lead by itself to a reduced melting temperature,

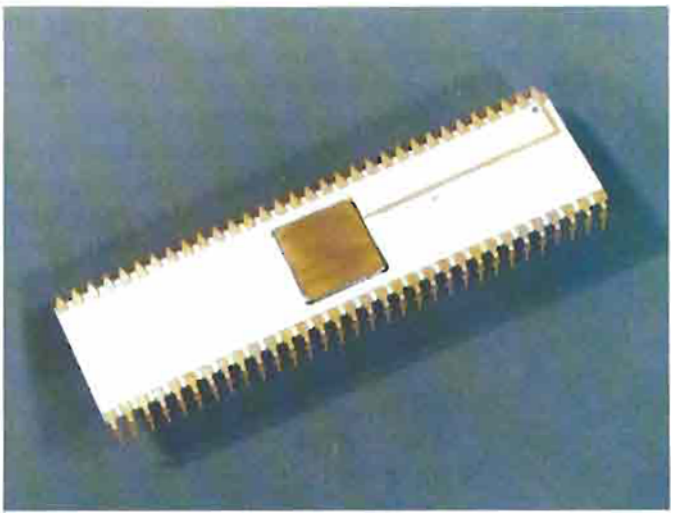


Fig. 3 The gold mounting pad on an integrated circuit package. The silicon integrated circuit chip is placed on the mounting pad to form the bottom attachment. (Photo courtesy of Texas Instruments, Dallas, Texas)

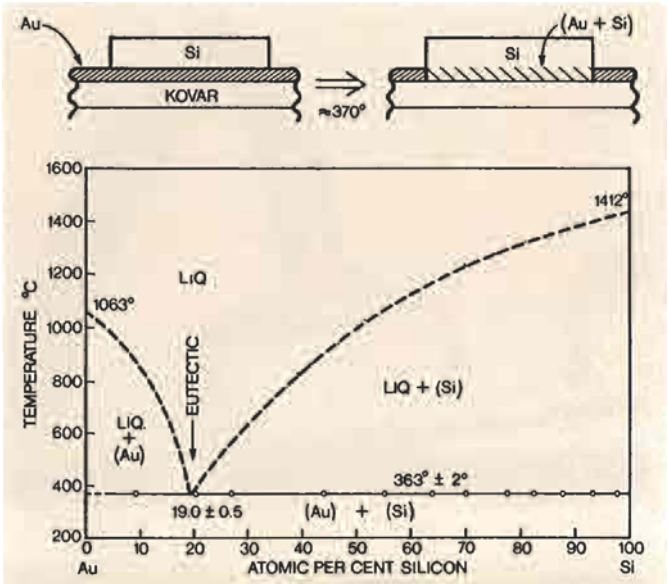


Fig. 4 The Au-Si phase diagram showing the eutectic temperature of 363°C and the composition with 19 atomic per cent silicon. The upper portion of the figure shows the method of attaching a silicon integrated circuit chip to the gold plated mounting pad shown in Figure 3

characteristic of a gold-silicon alloy. However, gold interacts with silicon at temperatures well below the eutectic. Such solid-phase reactions have been extensively reviewed (6, 7). Silicon can react with gold films to form an inter-diffused region and if the sample is heated around 370°C a liquidus is formed (see upper portion of Figure 4). Since only a limited thickness of gold plating is used only a negligible amount of the 250 μm thick silicon is consumed in forming the attachment. The presence of a resolidified gold-silicon alloy is evident in Figure 5 by the irregularly shaped dark-coloured region surrounding the silicon chip.

Dramatic demonstration of the reaction between gold and silicon at temperatures around 100 to 200°C is given by the growth of a thin silicon oxide layer on top of a gold film that has been deposited on a single crystal silicon substrate. As shown in Figure 6, if a sample is placed in an oxidizing ambient such as steam or even air a silicon oxide layer several hundred angstroms thick grows in less than one hour (8, 9). For gold layers one to two thousand angstroms thick the growth of the oxide follows a relationship of $t^{\frac{1}{2}}$ (t = time) that is typical of diffusion-limited processes. Other noble and near-noble metals such as silver and platinum also react with silicon. The transport of silicon through silver occurs at higher temperatures (9), approximately 400°C, than that through gold, and platinum forms a compound with silicon, platinum-silicide (6, 8). The striking feature of the formation of silicon oxide on gold-coated silicon is that in conventional processing steps the formation of silicon dioxide on silicon requires high temperatures (850-1 000°C).

The mechanisms involved in the low temperature oxide formation are shown in the upper portion of Figure 7. The first step in the process is the release of silicon atoms from the single crystal silicon lattice. Silicon is covalently bonded and has a high melting temperature so that an interfacial reaction is required to break the bonds. Gold diffuses interstitially in silicon and the presence of gold atoms at the surface is sufficient to disrupt the ordered array of silicon atoms. With even four monolayers of gold deposited on silicon, the interaction is sufficiently strong to form a disordered gold-silicon mixture even at room temperature (10). In the solid-phase, the equilibrium solubility of silicon in gold is small, less than 0.1 atomic per cent, and hence it is difficult to detect the presence of silicon in the outer region of a several thousand angstrom thick gold layer. However, the diffusivity of silicon in gold is high so that if one provides a sink for silicon at the outer surface of the gold film it is possible to detect the accumulation of silicon. The sink is provided by the presence of an oxidizing ambient because of the strong silicon oxygen reactions. The growth of the oxide is then determined by two diffusion processes, that of silicon through the gold layer and that of oxygen through the oxide layer. As in the case of the high temperature growth of silicon dioxide, SiO_2, the presence of water in the oxidizing ambient increases the oxidation rate (hence in Figure 6 the oxide thickness grown in steam at 100°C is comparable to that grown in dry oxygen at 200°C). For the present case of gold on silicon the oxide layer is porous — not as perfect as the conventional high temperature (900 to 1 000°C) grown SiO_2 layer — so that there is a ready path for the transport of oxygen.

The growth of the oxide layer has been studied by the use of Rutherford backscattering spectrometry (6, 7, 11). As shown in Figure 7 (insert in lower portion) an incident beam of collimated, monoenergetic helium ions is directed at the target. Most of the energetic particles penetrate into the target but a precisely-known fraction undergo large-angle, coulomb scattering from the target atoms. These large scattering events were known in the classic alpha particle scattering experiments in the period around 1910 and were the cornerstone for Rutherford's model of the atom; this is the origin of the name 'Rutherford backscattering' that is applied to this modern analytical technique. The additional word 'spectrometry' is used because measurement of the energy of the backscattered particles provides information on both the atomic mass and the depth distribution of the various target atoms within the sample. In the case shown in Figure 7, there are gold, silicon and oxygen atoms present in the near-surface region. Mass identification is provided by recoil kinetics — billiard-ball collisions — in which the amount of energy of the scattered helium ions is determined by the mass of the target atom. For true backscattering at 180°, the energy of the backscattered particle is given by the square of the ratio of the difference in target and helium atomic masses over the sum of their masses:

$$E = (M_T - M_{He}/M_T + M_{He})^2$$

This energy difference is a major effect; for example, with 2 MeV

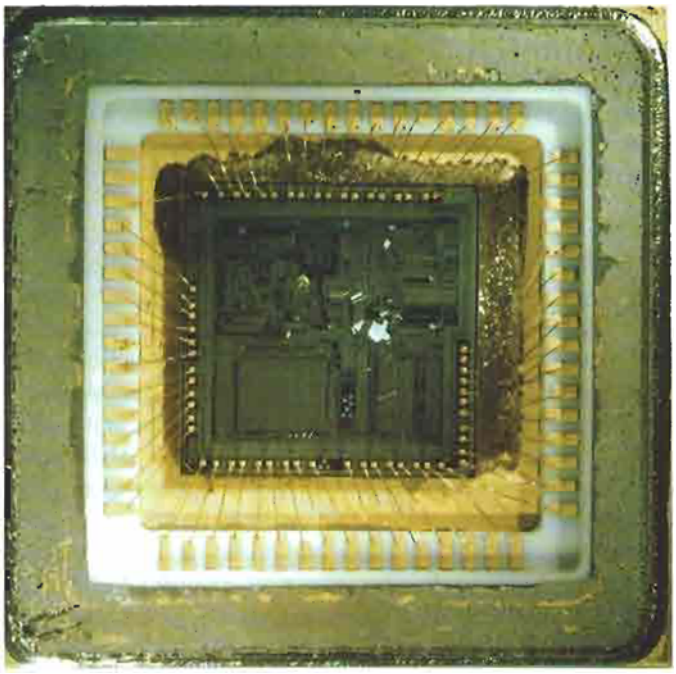


Fig. 5 Top view of a silicon integrated circuit chip after it has been attached to the gold plated pad on the package and the gold wires have been thermo-compression bonded. The dark-coloured irregular shaped region around the silicon chip is the resolidified Au-Si liquidus. (Photo courtesy of Texas Instruments)

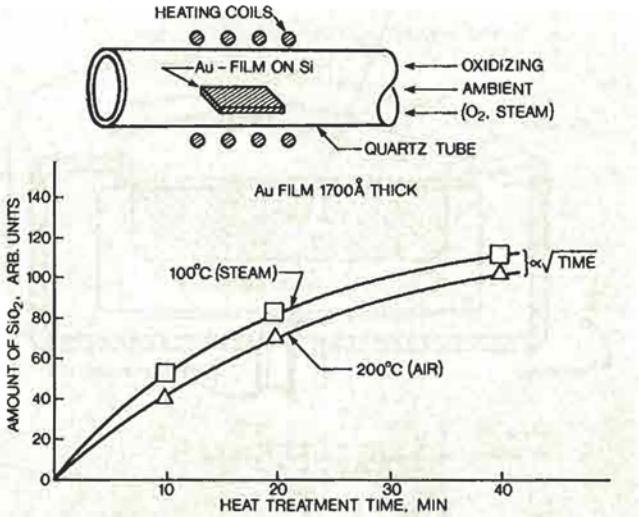
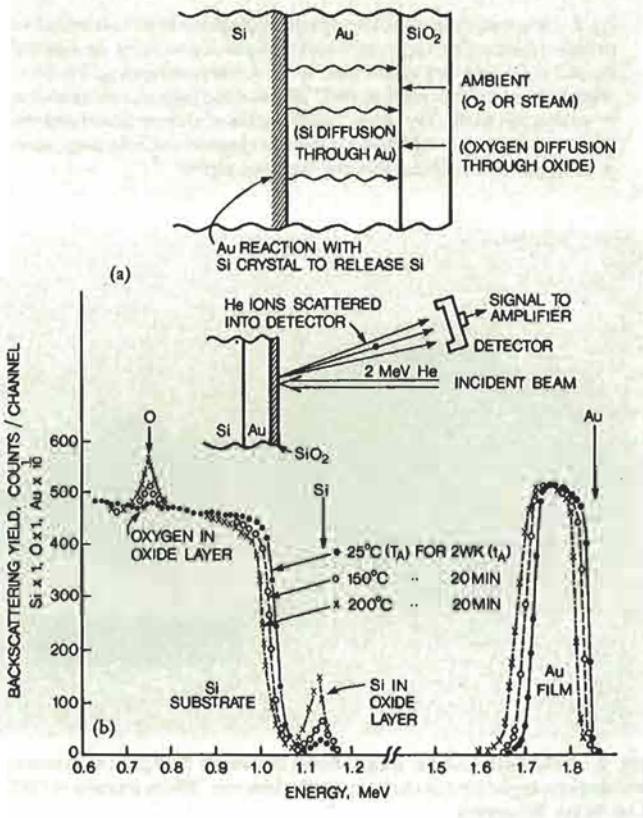


Fig. 6 Growth kinetics for the formation of a silicon oxide film on a gold film deposited on single crystal silicon and heated to temperatures below the Au-Si eutectic in an oxidizing atmosphere

Fig. 7(a) Schematic representation of the processes involved in low temperature formation of silicon oxide layers on a gold film deposited on single crystal silicon. (b) Rutherford backscattering spectroscopy measurements of oxide formation on a 90 nm thick gold film deposited on silicon



incident helium ions, the energy of helium atoms scattered from gold is more than twice that of particles scattered from oxygen atoms — a difference of over a million electron volts. The vertical arrows shown indicate the energies of helium ions scattered from gold, silicon and oxygen atoms on the surface. The other feature, the depth information, is provided by the energy lost by the incident particles as they penetrate the film — typical values range from 30 to 80 eV/ angstrom. Consider the signal from the gold film in the energy spectrum of Figure 7. The finite energy width is a measure of the number of gold atoms/cm² in the film. Energetic ions that penetrate the film and are scattered at the back interface of the film lose energy on their inward path, during the scattering event and on their outward path. For a thousand angstrom gold film, there is an energy difference of about 130 keV between particles scattered from the front and rear surfaces of the film. The energy loss values are tabulated (11) and the energy widths are almost directly proportional to the film thickness — a fact that makes Rutherford backscattering spectrometry a powerful technique for the analysis of thin film systems (4).

In the backscattering spectrum shown in Figure 7, the presence of the thin oxide layer on the surface of the gold film is indicated by both the downward shift in energy of the gold signal and the appearance of silicon and oxygen signals. The fact that the oxide layer is confined to the outer regions of the sample is given by the peaks in the silicon and oxygen signal. The low solubility of silicon

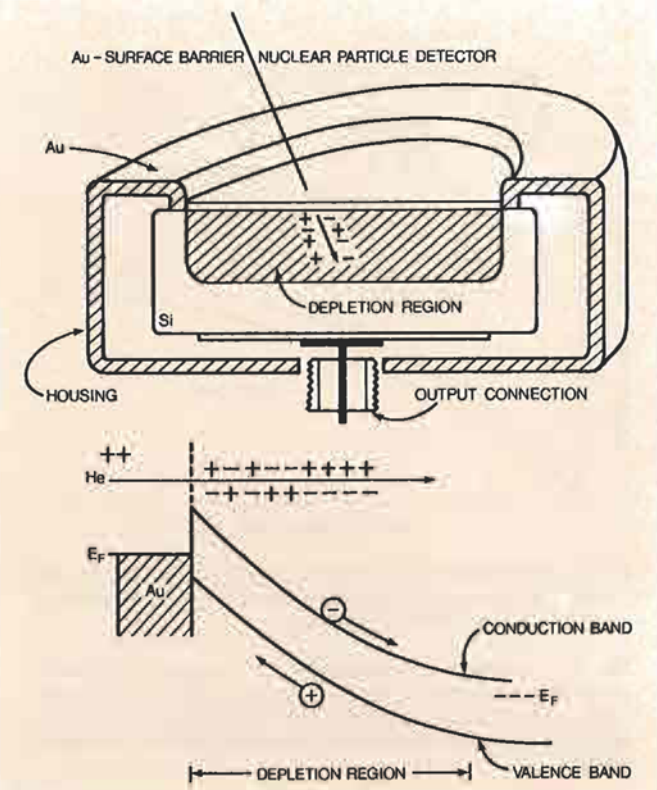


Fig. 8 Schematic diagram of the operation of a gold surface barrier nuclear particle detector. The upper portion of the figure shows a cutaway sketch of the silicon disc with its gold film mounted in the detector housing. The lower portion shows an alpha particle, He^{2+} ion, forming holes and electrons over its penetration patch. The energy band diagram of a reverse biased detector (positive polarity on *n*-type silicon) shows the electrons and holes swept apart by the high electric field within the depletion region

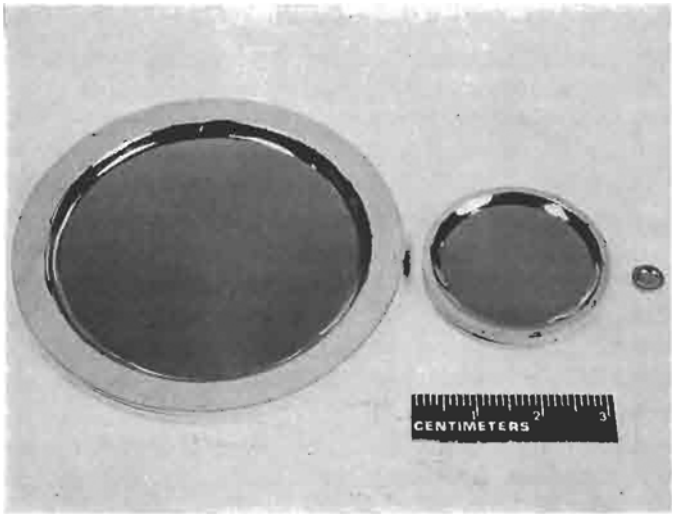


Fig. 9 Gold surface barrier silicon diodes on ceramic discs prior to mounting in housings for application as nuclear particle detectors. (Photo courtesy of ORTEC, Oak Ridge, Tennessee)

in gold is brought out by the small signal (at energies of around 1.1 MeV) that corresponds to scattering from silicon atoms within the gold film. The ratio of silicon to oxygen atoms in the oxide layer can be found from integrating the area under the silicon and oxygen peaks in the spectrum and then correcting from the ratio of scattering cross-sections.

Rectifying Contacts to Semiconductors

The particle detector shown in Figure 8 is a gold-surface barrier nuclear particle detector. This is an example of the other major utilization of gold as a contact to semiconductors — in this case the formation of a rectifying contact. Before we discuss the formation of the rectifying contact and its application in semiconductor integrated circuits we will give an overview of the nuclear particle detector. It was discovered nearly thirty years ago (12, 13) that a gold layer on silicon or germanium could form an active region within the semiconductor that would respond linearly to the energy of an incident particle — in effect producing an alpha particle spectrometer. These detectors made an immediate impact on nuclear physics because of their compact size — centimetres as compared to the massive magnetic spectrometers — as well as their fast, linear response. These detectors became the cornerstone of the nuclear electronics industry as they promoted the development of the modular instrumentation used today.

The operation of these detectors is straightforward as indicated in the schematic diagrams in Figure 8. The cutaway drawing in the upper portion shows the detector consisting of a disc of high purity silicon mounted in a housing with a thin layer of gold deposited on the top of the silicon. Under reverse bias polarity applied through the output connection to the back contact, a region of high electric field, the depletion region, is produced in the silicon under the gold layer. Depending upon the purity of the silicon and the magnitude of the applied bias voltage, the width of the depletion region can extend from tens of micrometres to nearly millimetres in thickness. The penetration depth of the alpha particles is typically only a few micrometres and hence they lose all their energy within the depletion region. As shown in the lower portion of the figure, the penetration of an alpha particle into silicon produces holes and electrons along the track of the particle. A 4MeV alpha particle produces in excess of a million electrons and holes. Because the gold layer is thin, less than 100μg/cm², the dominant energy loss is within the silicon and the number of charge carriers produced is proportional to the energy of the alpha particles. As shown in the energy band diagram of the reverse-biased detector, the electrons and holes created within the depletion layer are swept apart by the electric field within the depletion layer. The motion of the carriers produces a current pulse which appears as a fast rising voltage pulse across the output load resistor. The height of the voltage pulse is directly proportional to the energy of the incident particle. Pulse height analyzers are used to display the energy spectrum of the particles.

The surface barrier detectors come in many sizes and configurations. They have been made in annular configurations (with a central hole for the incident beam), mounted in hypodermic needles for medical applications, and have been made in 'checkerboard' style with multiple detectors formed on one silicon disc for use in angular resolved nuclear physics studies. The different sizes of the conventional detectors are exemplified by the gold covered silicon discs shown in Figure 9. These are ceramic mounts, that are later placed in the detector housing.

Energy or Schottky Barrier Contacts

The key feature in the surface barrier nuclear particle detector is the formation of an energy barrier or Schottky barrier at the gold/*n*-type semiconductor interface. It is the same barrier formation that is responsible for the operation of the gold Schottky barrier solar cell discussed by Williams in an earlier issue of *Gold Bulletin* (1). The presence of an energy barrier between the gold and semiconductor prevents the flow or injection of electrons from the gold into the semiconductor. Consequently, as illustrated in Figure 8, one can apply a positive voltage (reverse bias polarity) to the *n*-type semiconductor and establish a large electric field of the order of 10^4 V/cm without a concommitent flow of electrons. This energy barrier forms the blocking or rectifying contact.

The Importance of Gold Schottky Barriers

In order to minimize the current flow in the reverse bias or blocking direction, it is desirable to maximize the barrier height. Gold, of all the common metals, displays the highest barrier heights on *n*-type semiconductors (14). For example, Figure 10 shows the barrier heights ϕ_B of gold, aluminium and silver on silicon and germanium (15).

The gold contact produces the largest barrier height at a value somewhat greater than three-quarters of the band gap. All the three metals form eutectic systems with silicon and germanium and the barrier heights are plotted versus eutectic temperature to emphasize the correlation between Schottky-barrier height and eutectic temperature, a correlation that has also been found in silicides in contact with silicon (15). The factors which determine barrier heights and therefore the dominant role played by gold in Schottky barrier devices are still under active study. This situation holds in spite of the fact that an asymmetrical electrical conduction was observed as long ago as 1874 across a metal-semiconductor couple (16). It was some sixty-five years later, in 1939, that an interpretation of the rectifying behaviour of such contacts was given by Mott (17) and Schottky (18). The concept of Mott was that the rectifying barrier was due to the difference in the work-function of the metal and the electron affinity of the semiconductor. In the period of over 40 years since this early theory was put forward an impressive amount of experimental data has been collected. The data can generally be characterized as exhibiting a large spread in the observed barrier height values. It is now recognized that the cleanliness and perfection of the metal-semiconductor interface is a critical factor that influences the barrier height. The spread in barrier height values is attributed to differences in interface cleanliness. A density of surface states equivalent to a thousandth of a monolayer is sufficient to pin the barrier height. For example the presence of a thin oxide layer between the metal and silicon surface is sufficient to give barrier heights that are nearly independent of the metal. The data in Figure 10 were obtained with carefully cleaned interfacial regions.

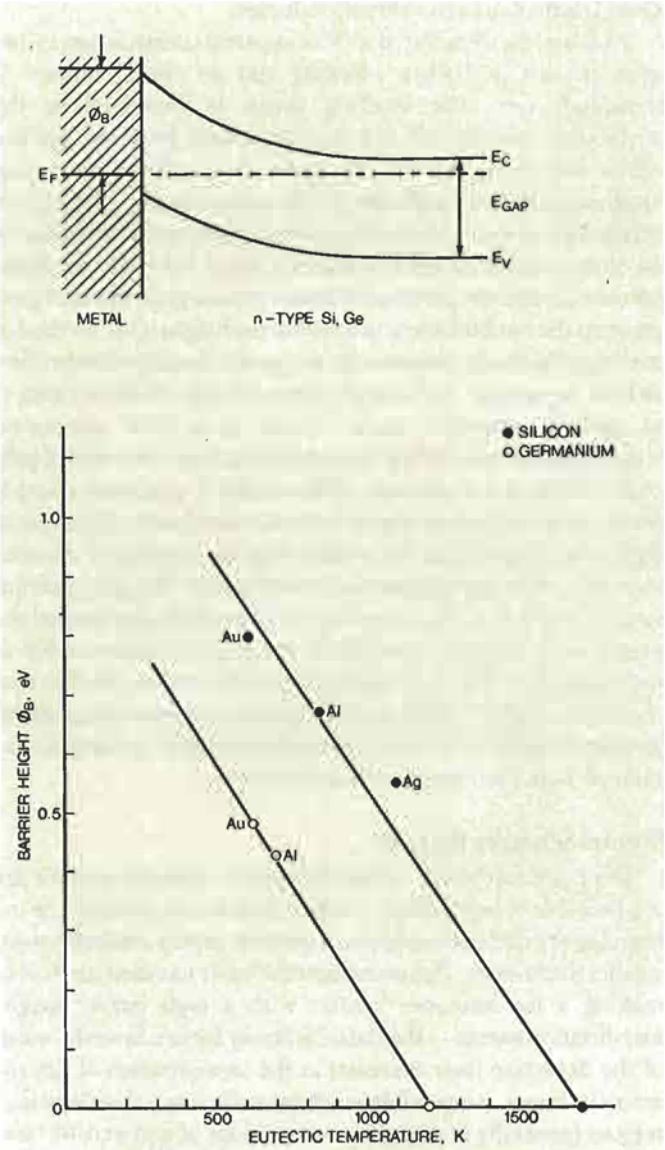


Fig. 10 Schottky Barrier heights ϕ_B versus eutectic temperature for metal-silicon and metal-germanium systems which have a simple eutectic phase diagram such as that shown in Figure 4. (Adapted from Ottaviani *et. al.* (15))

Gold Ohmic Contacts to Semiconductors

At this point we are faced with an apparent contradiction in that gold can act as both a blocking and an ohmic contact to semiconductors. The blocking action is illustrated by the application to solar cells and nuclear particle detectors, and the ohmic nature by the use of a gold-silicon alloy for the chip attachment shown in Figure 4. The existence of a gold-silicon mixture in contact with the silicon crystal ensures the formation of an ohmic contact as gold produces a major reduction in carrier lifetime (2) and the presence of an intermixed gold-silicon region prevents the establishment of a full barrier height. One method of making gold ohmic contacts to an *n*-type semiconductor is therefore to heat the sample. For example in studies (19) of ohmic contacts to gallium arsenide, GaAs, which is a III-V compound semiconductor used for high speed devices, heat treatment of gold coated GaAs at temperatures of 400 to 600°C produced a deeply penetrating component of gold in the semiconductor. A disordered region was found near the surface with the amount of disorder increasing with process time and temperature. The gold-gallium eutectic is at 339°C (5). Scanning electron microscopy showed the presence of rectangular pits after the samples were alloyed at 400°C indicative of the formation of localized melt erosion. The fact that the contact resistance decreased for process temperatures of 400°C and above, again shows the effectiveness of a gold-semiconductor mixture in the formation of ohmic contacts.

Tunnel Schottky Barriers

Deep pits formed by contact formation above the eutectic are inadmissible in high density integrated circuit applications. As the lateral device dimensions decrease, junction depths also scale toward smaller thicknesses. This introduces the other standard method of making a low-resistance contact with a high barrier height metallization system — the tunnel Schottky barrier. Since the width of the depletion layer decreases as the concentration of dopant atoms increases, it is possible to achieve sufficiently thin depletion regions (generally at dopant concentrations of between 10^{19} and 10^{20} atoms/cm^3) so that the electrons can tunnel through the barrier and hence the blocking action of the high barrier is obviated. Such high dopant concentrations are generally achieved in semiconductor structures by the use of ion-implantation techniques. In this case one uses photoresist and masking techniques to expose selected areas of the semiconductor. The sample is then implanted with dopant atoms at energies of around 100 KeV with all but selected areas masked from the ion beam. We will illustrate the use of these techniques for the formation of both blocking and ohmic contacts on GaAs field effect transistors.

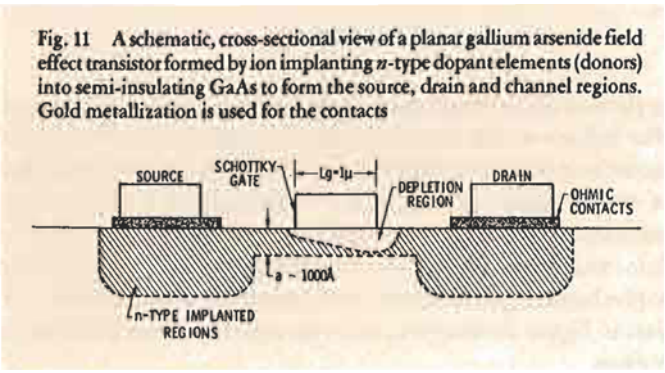


Fig. 11 A schematic, cross-sectional view of a planar gallium arsenide field effect transistor formed by ion implanting *n*-type dopant elements (donors) into semi-insulating GaAs to form the source, drain and channel regions. Gold metallization is used for the contacts

Gold in Devices Based on GaAs

Gallium arsenide is currently under intense study for development of high speed transistors for microwave and other high frequency applications. The mobility of electrons in GaAs is nearly a factor of ten greater than that in silicon and hence for the same device dimensions GaAs would display superior high frequency permanence as compared to silicon devices. Yet, silicon has a pronounced advantage over GaAs in that its process technology — diffusion, oxidation and contact formation — has been honed to a fine art. Over the past twenty years, silicon has been used in integrated circuits because of the manufacturing capability and production yields in silicon devices. In device research, GaAs devices have shown dramatic improvements due to the development of epitaxial growth techniques and the use of ion implantation. Gold contact metallurgy has been intimately tied to the development of these GaAs structures.

The basic configuration of a GaAs planar field effect transistor is shown in Figure 11. In this case the structure is formed on semi-insulating GaAs so that all the current paths are confined to the ion implanted regions. In the fabrication process, the first step is to implant a shallow layer about one thousand angstroms thick to form the channel region that will connect the source and drain for the transport of electrons. After another masking step, the source and drain are implanted with a high concentration of dopant atoms so that low resistance contacts can be formed — the tunnel barrier contact concept. The sample is then annealed to remove the lattice disorder caused by ion implantation and to cause the dopant atoms to become electrically active.

Once the basic structure with source, drain and channel is formed, the gold metallization process becomes the key to the successful fabrication of a working transistor. The ohmic contacts are deposited and heat treated. The present metallurgy utilizes gold-germanium alloys because it has been found that lower resistance contacts are formed with about twenty atomic percent germanium in the gold (14, 19). Although there is no direct evidence, it is believed that the germanium becomes incorporated in the GaAs lattice during heat-treatment and forms a high *n*-type dopant concentration immediately adjacent to the metallic contact interface. Other metals eg. nickel or platinum have been also incorporated at about 10 atomic per cent to improve contact uniformity.

After a low resistance current path between source and drain has been assured, the Schottky barrier gate metal is deposited. The gate is operated under reverse bias conditions so that the resistance of the channel can be modulated by changes in the gate voltage — which in turn changes the thickness of the depletion region. The channel thickness modulation must be achieved without having excessive current flow through the gate contact, hence the barrier height is a key parameter. The gate depletion region excludes electrons (the gate is biased with a negative polarity) and hence restricts the current in the channel. Since a high Schottky barrier height is required to establish an effective depletion region with low leakage currents, gold again is the obvious choice. In this case, other metals are used with gold in the gate metal layer to ensure uniformity and adhesion.

Gold has the additional advantage that it is easy to deposit and sputter-etch in the submicron line-width geometries required for high frequency devices. Figure 12 shows a gold-based metallization field effect transistor made with large source and drain contacts (left and right side) and two triangular shaped connections to the gate. As indicated in the lower portion of the figure, the gate is less than 1 μm across. These small gate dimensions are required for high frequency applications. It is important to emphasize that it is the versatility and ease of fabrication available when using gold that has led to the widespread use of gold metallization in such high frequency Schottky barrier field effect transistors.

For integrated circuit applications such as that shown in Figure 13, not only must one form ohmic contacts and Schottky barriers but also first level interconnects between devices, insulating layers. Second and third level interconnects leading to other portions of the chip must also be provided. Gallium arsenide integrated circuits have been made successfully with gold-metallization.

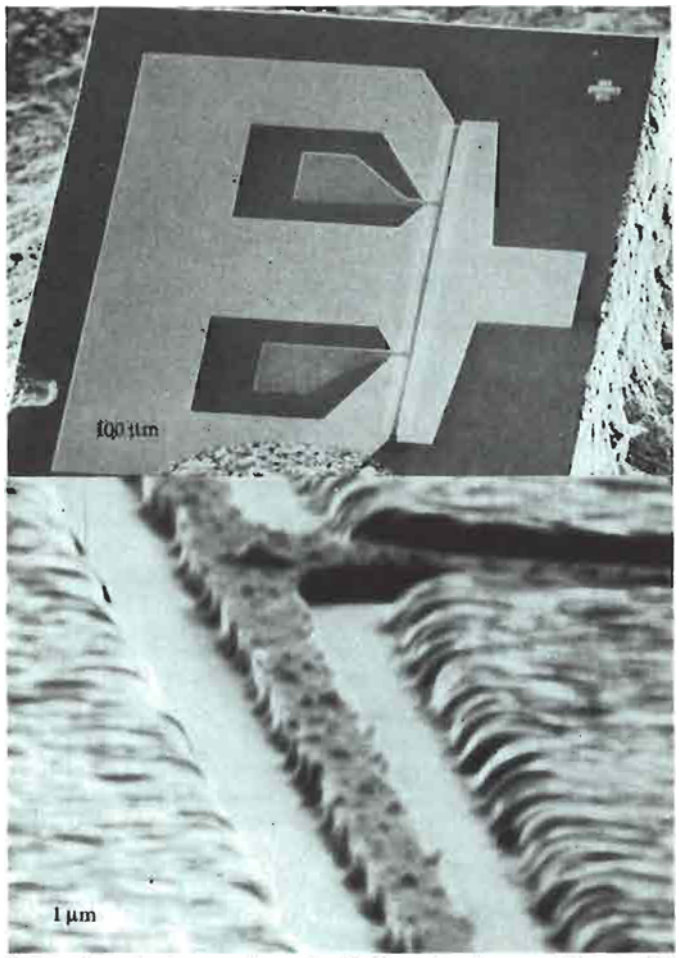


Fig. 12 Scanning electron micrographs of gold metallization on a gallium arsenide field effect transistor. The horizontal lines in the left corners show the distance scale. The lower portion of the figure shows the narrow gate that is required for high frequency operation. (Photo courtesy of Dave Woodard, Cornell University)

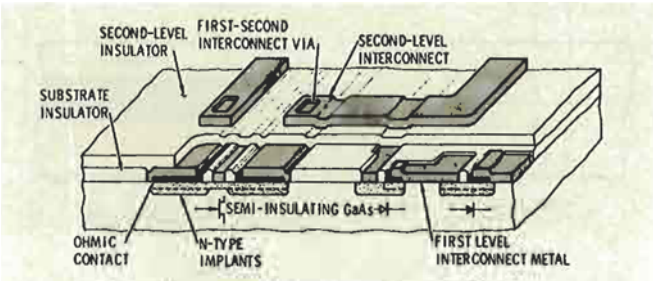


Fig. 13 Schematic cutaway drawing of a gallium arsenide integrated circuit formed by ion implantation and gold metallization on a semi-insulating substrate. (Sketch courtesy of Rockwell International Research Center)

Ion Beam Mixing

Efforts continue to be made to improve the uniformity of the gold contacts. One approach that promises to have applications to contact formation in III-V compound semiconductors, is the use of energetic ion beams to induce interface mixing. In the eutectic systems, the concept has been demonstrated by implanting energetic rare gas ions through a thin layer of gold deposited on a silicon single crystal substrate (20). As shown in the upper portion of Figure 14, the penetration of the ions through the interface produces a layer by layer growth of a gold-silicon mixture with 28.5 atomic per cent silicon. Rutherford backscattering measurements showed that the alloys are rather uniform in composition and transmission electron microscopy showed that the alloy was amorphous. With heat treatment the amorphous phase transforms around 100°C to a metastable crystalline (hexagonal lattice structure) compound Au_5Si_2 as indicated in the phase diagram. The metastable structure decomposes at temperatures around 180°C into the equilibrium gold and silicon two-phase system. Metastable phases of Au-Si (shaded region) have also been formed by rapid quenching. The properties of ion-induced amorphous alloys are quite similar to those produced by rapid quenching of gold-silicon mixtures except that the ion-induced alloy has a well-defined composition and exhibits a higher stability with respect to the thermal transformation to the metastable crystalline phase.

Ion beam mixing was originally introduced as a low-temperature

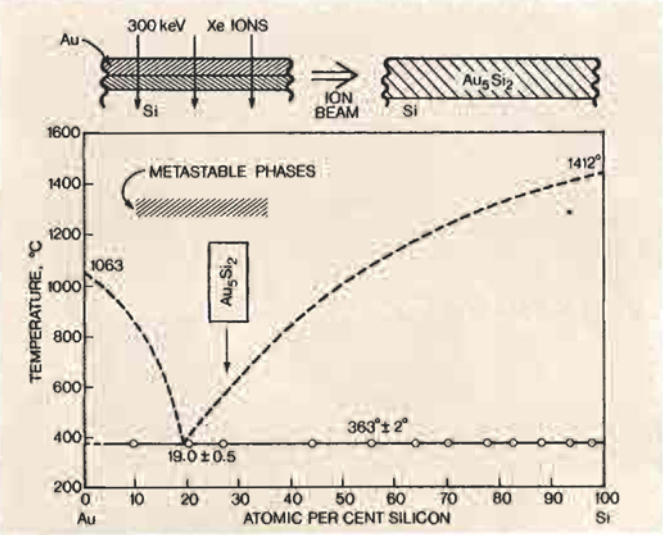
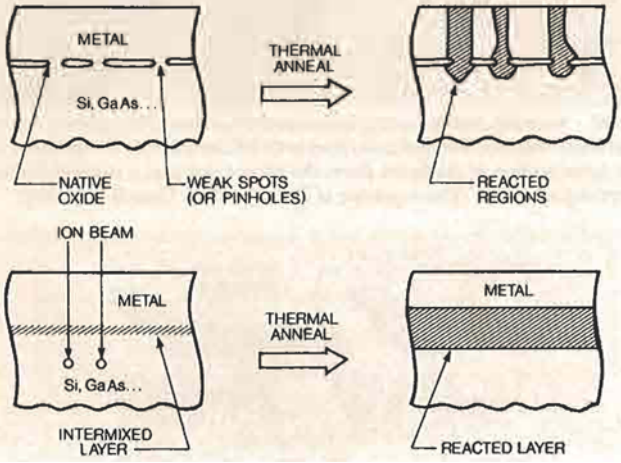


Fig. 14 Formation of metastable Au-Si alloys by ion beam mixing in which a beam of energetic ions, Xe ions in this case, penetrates the interface between the gold film and silicon substrate to form an amorphous Au-Si alloy with 28 atomic per cent silicon. Heat treatment at 100°C produces a metastable crystalline phase, Au_5Si_2

Fig. 15 Reactions between deposited metal and semiconductor-substrate. (a) The presence of non-uniform interfacial contaminants leads to laterally non-uniform reactions. (b) Ion beam mixing produces an intermixed layer that leads to uniform contact formation in subsequent thermal annealing



process step to form metastable phases due to the fast-quenching that results from the rapid dissipation of heat from the collision cascade around the ion track. Indeed it was found that amorphous platinum-silicon compounds could be formed that transformed into metastable crystalline compounds (Pt_2Si_3 and Pt_4Si_9) that exhibited superconducting properties (21). However the ability to form uniform mixtures at the metal-semiconductor interface opens up new possibilities in device fabrication.

For example, with thermal reactions, contaminants or oxide layers at the metal-semiconductor interface can impede or cause irregular interfacial reactions as shown in Figure 15. The influence of interface contamination can largely be overcome by the penetration of energetic ions through the interface. For example, thermal annealing after interface mixing leads to the growth of uniform silicide layers (22). With the widespread use of ion implantation as a means of introducing dopant atoms and with the possibility of using ion mixing, one can envisage the formation of reliable ohmic contacts and shallow *p-n* junctions by the implantation of dopant atoms through a metal overlayer followed by heat treatment. The technique lends itself naturally to device applications where the thermal treatment also has the function of removing the damage caused by the ion and electrically activating the implanted dopant atoms. Not only have such concepts been applied successfully to form contacts in silicon devices, they have also been utilized to form uniform, low-resistance contacts with gold layers on GaAs (23).

Conclusion

This article has attempted to show that the past, present and future of semiconductor device production and development has been, and is likely to be, tied to the use of gold contacts. Gold will continue to hold a place in the semiconductor electronic industry. From an economic standpoint, there have been efforts for years to reduce the gold content in contacts to semiconductors but gold has been difficult to displace due to its ductility, corrosion resistance, electrical conductivity and barrier height. One can anticipate continued usage of gold as ohmic contacts and Schottky barriers in compound semiconductors such as GaAs because of the versatility of gold metallization in device fabrication.

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